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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/723,377

11/26/2003

Tam Minh Tran

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05/02/2006

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EXAMINER

EHNE, CHARLES

ART UNIT

PAPER NUMBER

2113

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,377	TRAN ET AL.	
	Examiner	Art Unit	
	Charles Ehne	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11, 12, 14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-10 and 16-18 is/are allowed.
- 6) ☒ Claim(s) 11, 12, 14 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 14-18 are to be renumbered 13-17.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14-15 (original) recites the limitation "selected from the group" in line 4.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11,12,14 and 15 (original) are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (6,457,108) taken in view of Chih (2003/0154437).

As to claim 11, Hsu discloses a memory device with repair capability comprising:
a supply voltage (column 4, lines 49-52);
power control logic connected to the supply voltage (column 4, lines 46-49);
at least one switch connected to the supply voltage (column 4, lines 46-49);
a memory array connected to the at least one switch (column 5, lines 44-50); and
peripheral logic connected to the at least one switch (column 4, lines 56-57).

Hsu discloses data registers connected to the supply voltage and the at least one switch, wherein the at least one switch is operational to remove power to the peripheral logic, the memory array and selected portions of the data registers in response to power control logic signals such that data is retained in the registers subsequent to power down of the peripheral logic, the memory array, and the selected portions of the repair data registers (column 9, lines 47-50), but fails to disclose that the data is memory repair data.

Chih does disclose that non-volatile memory can be utilized to store information necessary to repair defective memory arrays (page 1, ¶ 0010, lines 1-5). Chih also discloses that memory repairing data is generally read out of a volatile latch array after the computer system is powered up (page 1, ¶ 0010, lines 5-7).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hsu's method of retaining data during removal of power with Chih's method of retaining memory repair data. A person of ordinary skill in the art would have been motivated to make the modification because Hsu's provides a method to ensure maximum data retention (Hsu: column 1, lines 16-18) which would allow further fault tolerance for consistent data retention when reading memory repair data.

As to claim 12, Chih discloses the memory device according to claim 11, wherein the repair data registers comprise retention latch circuitry operational to store and maintain the memory repair data (page 1, ¶ 0010, lines 5-7).

As to claim 14, Hsu discloses a memory device with repair capability comprising:
a supply voltage (column 4, lines 49-52);
power control logic connected to the supply voltage (column 4, lines 46-49);
at least one switch selected from the group consisting of a Vss footer switch, and a Vdd header switch (column 4, lines 54-60);
a memory array connected to the at least one switch (column 5, lines 44-50); and
peripheral logic connected to the at least one switch (column 4, lines 56-57).

Hsu discloses data registers connected to the supply voltage and the at least one switch, wherein the at least one switch is operational to remove power to the peripheral logic, the memory array and selected portions of the data registers in response to power control logic signals such that data is retained in the registers subsequent to power down of the peripheral logic, the memory array, and the selected portions of the repair data registers (column 9, lines 47-50), but fails to disclose that the data is memory repair data.

Chih does disclose that non-volatile memory can be utilized to store information necessary to repair defective memory arrays (page 1, ¶ 0010, lines 1-5). Chih also discloses that memory repairing data is generally read out of a volatile latch array after the computer system is powered up (page 1, ¶ 0010, lines 5-7).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hsu's method of retaining data during removal of power with Chih's method of retaining memory repair data. A person of ordinary skill in the art would have been motivated to make the modification because Hsu's provides a method to ensure maximum data retention (Hsu: column 1, lines 16-18) which would allow further fault tolerance for consistent data retention when reading memory repair data.

As to claim 15, Chih discloses the memory device according to claim 14, wherein the repair data registers comprise retention latch circuitry operational to store and maintain the memory repair data (page 1, ¶ 0010, lines 5-7).

Allowable Subject Matter

Claims 1-10 and 16-18 (original) are allowed.

The following is an examiner's statement of reasons for allowance:

Claim 1 discloses maintaining power to the power control logic and repair data registers during loss of power to the E-fuse farm and associated memory module circuitry, such that the memory repair information is retained by the memory module during the loss of power to the E-fuse farm and associated memory module circuitry.

Claim 6 discloses maintaining power to the memory module power control logic and memory module repair data registers during loss of power to the E-fuse farm and associated memory module circuitry, such that the memory repair information is retained by the memory module during the loss of power to the E-fuse farm and associated memory module circuitry.

Claim 16 discloses at least one memory module comprising repair data registers, wherein the at least one memory module operates to maintain memory repair data in the repair data registers in response to power management control logic signals during loss of power to portions of the device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."


Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Ehne whose telephone number is (571)-272-2471. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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